



Attorney Docket No. 5646-81

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Proebsting et al.
Serial No.: 10/643,208
Filed: August 18, 2003
For: INTEGRATED CIRCUIT DEVICES HAVING PRECISION DIGITAL DELAY LINES
THEREIN

Group Art Unit: 2812
Examiner: To Be Assigned
Confirmation No.: 4050

Date: December 15, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on Form PTO-1449, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the waiver by the U.S. Patent and Trademark Office of requirements under 37 C.F.R. § 1.98(a)(2)(i) for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003.

It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

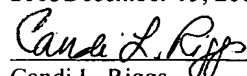
Respectfully submitted,


Grant A. Scott
Registration No. 36,925

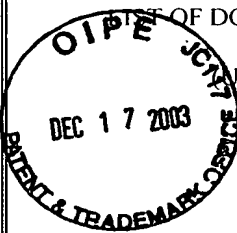
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 15, 2003/December 15, 2003.


Candi L. Riggs

Date of Signature: December 15, 2003

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office				Attorney Docket Number 5646-81		Serial No. 10/643,208	
<div style="display: flex; align-items: center;"> <div style="text-align: center; margin-right: 10px;">  </div> <div> LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary) </div> </div>				Applicants: Robert J. Proebsting			
				Filing Date: August 18, 2003		Group 2812	
U. S. PATENTS & PATENT APPLICATION PUBLICATIONS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1	6,593,786	7/15/03	Jung	327	158	
	2	6,586,978	7/1/03	Stief	327	158	
	3	6,584,021	6/24/03	Heyne et al.	365	194	
	4	6,539,072	3/25/03	Donnelly et al.	375	371	
	5	6,518,807	2/11/03	Cho	327	158	
	6	6,504,408	1/7/03	von Kaenel	327	158	
	7	6,501,328	12/31/02	Gauthier et al.	327	551	
	8	6,501,312	12/31/02	Nguyen	327	161	
	9	2003/0154447	8/14/03	Gauthier et al.	716	2	
	10	2003/0154417	8/14/03	Drexler	713	400	
	11	2003/0151433	8/14/03	Takai	327	158	
	12	2003/0141910	7/31/03	Reindl	327	158	
	13	2003/0117194	6/26/03	Lee	327	158	
	14	2003/0117193	6/26/03	Lee	327	158	
	15	2003/0108139	6/12/03	Jung	375	376	
	16	2003/0099321	5/29/03	Juan et al.	375	376	
	17	2003/0095009	5/22/03	Gomm et al.	331	57	
	18	2003/0094984	5/22/03	Weis et al.	327	182	
	19	2003/0090296	5/15/03	Yoo	327	12	
	20	2003/0071668	4/17/03	Starr	327	157	
	21	2003/0067335	4/10/03	von Kaenel	327	158	
	22	2003/0058014	3/27/03	Krishnamurty	327	158	
	23	2003/0052719	3/20/03	Na	327	158	

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FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation Yes No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	24	U.S. Patent Application No. 10/094,101, entitled <i>Apparatus and Method for Generating a Compensated Percent-of-Clock Period Delay Signal</i> , Inventor: Cesar A. Talledo, Filed March 8, 2002, 26 pages					

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